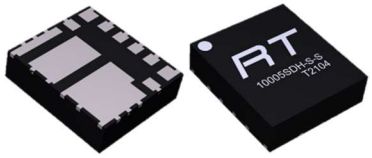
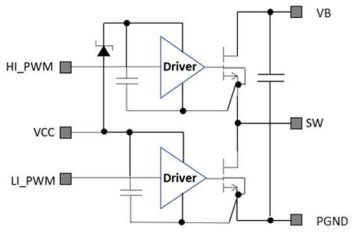
Features

- Complete R_{DSON}= 5.6mΩ Half-Bridge GaN-Based power stage
- Maximum Output Current 14A.
- GaNCooling™ technology by Bottom Side Cooling
- Low FOM for low Switching Loss at 1MHz+
- Complete solution within 7.5mm x 6.7mm x 1.95mm Footprint
- Dual PWM operation
- Fast Rise/Fall Times and low Propagation Delay
- Reverse Current capability and Zero Q_{RR}
- Moisture Sensitivity Level 3 (260°C)

QFN 7.5x6.7mm² System in Package (SiP)



Simplified Schematic



Typical Applications

- 48V Datacenter board power delivery
- Power stage for DC-DC Converters
- 48V Mild Hybrid DC-DC Converter and BSG
- High-performance Class D Audio systems
- Motor Drive Inverter

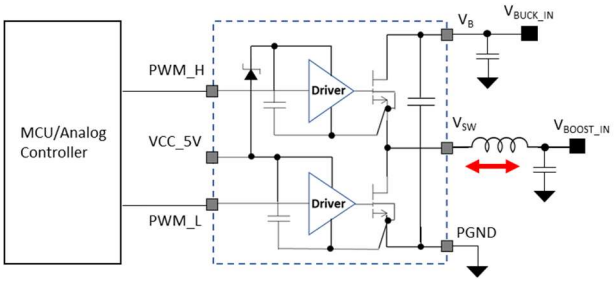
Description

RT100 DrGaN (Driver+GaN Half Bridge) Series are Fully Integrated GaN Half-Bridge power stages for multiple Applications in Datacenter, Motor Driver, and Consumer segments. These DrGaN are small-footprint, easy-to-design, and serve as a “drop-in” solution for board power. RT100 DrGaN Series couples world-class GaN performance from EPC eGaN™ to Raytrons GaNCooling™ embedded modules that GaNCooling™ technology is a patented construction embeds all components without using bond wires, minimizing inductance, achieving ultra-low voltage spikes on gate and switch nodes, and minimizing RFI. The high dV/dt immunity, <1nH loop inductance and low thermal resistance to provides highest level of Power Density allowing designer simple, and quick to design high power density product.

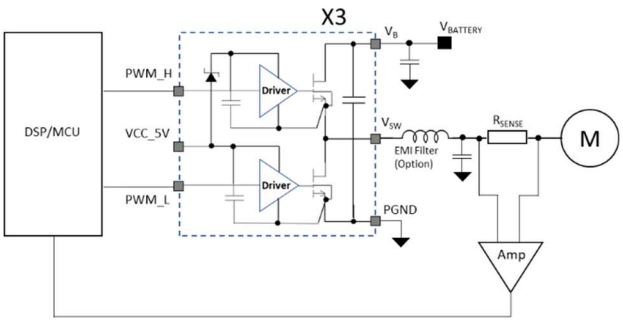
Typical Application Circuit

A synchronous buck or boost topology with V_{CC} connected to a 5-V regulated supply. Power loop (loop impedance from VB capacitor to GND) PCB layout is critical, designer can refer to the PCB layout consideration section to selection dual-loop or thermal enhanced PCB layout for various applcations

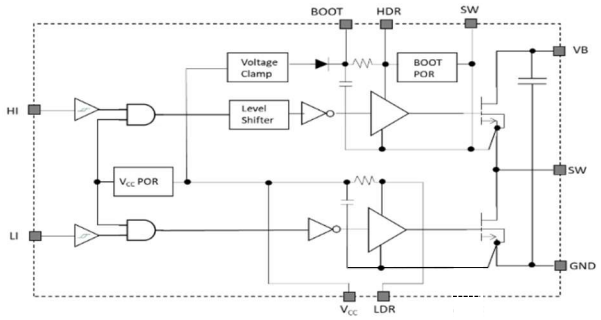
Bi-directional Buck/Boost DC/DC Conversion



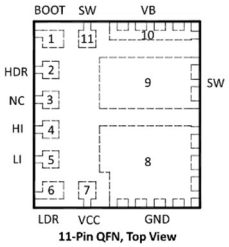
3-Phase Motor Driver



Block Diagram



Pinout Table



11-Pin QFN, Top View

Pinout		I/O Type	Description and Operation
#	Name		
1	BOOT	Supply	Floating high side gate driver supply that connected inside
2	HDR	-	Option. Parallel a resistor between HDR and BST to speed up dv/dt falling time at SW node, the resistor value =2Ω is recommended if necessary.
3	NC	-	No Connection
4	HI	Input	Low Side PWM Input
5	LI	Input	High side PWM Input
6	LDR	-	Option. Parallel a resistor between LDR and VCC to speed up dv/dt rising time at SW node, the resistor value =2Ω is recommended if necessary
7	VCC	Supply	Low Side Driver Supply Voltage. Connect a 5V regulated Voltage.
8	GND	Power GND	Connect to PCB Ground thru multiple Via's
11,9	SW	Power Output	Half-Bridge power stage output (switching node)
10	VB	Power Input	Supply voltage to half-bridge power stage (buck-mode)

Absolute Maximum Ratings (T_{CASE} = 25 °C)

Permanent device damage may occur if Absolute Maximum Ratings are exceeded.

- VB to GND, VB to SW, SW to GND ---------- 85V
- VCC to GND ---------- 7V
- LDR, LI, HI to GND ---------- 7V
- HDR, BST to GND ---------- 85V+VCC

Thermal Characteristics

The Surface Mount Device (SMD) with Bottom-side Cu Pads for Surface Mount PCB attach. $R_{\_JUNC-AMB}$ value based on recommended Via Pattern with multi-layer FR4 PCB. No Airflow (zero LFM) and no Top-side Heat Sink required to meet $R_{\_JUNC-AMB}$ (Conduction Heat Transfer). It is much more effective and competitive thermal design.

- Maximum Thermal Resistance (Junction to Board), R_{Θ_JB}, ---------- 1.1 °C/W
- Thermal Resistance (Junction to Ambient), R_{Θ_JA}, ---------- 8.4 °C/W
- Maximum Soldering Temperature (MSL3 rated), T_{Solder} ---------- 260°C

Normal Operation Conditions

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Nominal VB Range	V_{B_Nom}	6.2		80	V	
Nominal SW Range	$SW_{\_Nom}$	0.9		80	V	
Nominal V_{CC} Range	V_{CC_Nom}	4.5	5	5.5	V	
Nominal I/O Voltage	V_{IO_Nom}			5.5	V	
Continuous I_{OUT}	I_{OUT_Nom}		14	15	A	T_{JUN}=100°C
Operating Temp	$T_{OPER.}$	-40		105	°C	

Electrical Specifications

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Drain-Source On Resistance	$R_{DS,ON}$		5.6	7.0	m Ω	H/S and L/S GaN Devices
Source-Drain Forward Voltage	V_{SD}		1.7		V	I_S = 0.5 A, V_{GS} = 0 V
Input Capacitance	C_{ISS}		767	1076	pF	V_{DS} = 50 V, V_{GS} = 0 V
Reverse Transfer Capacitance	C_{RSS}		3			
Output Capacitance	C_{OSS}		295	443		
Source-Drain Recovery Charge	Q_{RR}		0		nC	
Gate Resistance	R_G		2.6		Ω	
Bootstrap capacitance	C_{BST}	80	100		nF	DC-Bias=0V
V_{CC} capacitance	C_{VCC}	80	100		nF	DC-Bias=0V
Switching Frequency	F_{SW}	18		1000	kHz	
Propagation Delay	$T_{PD(H,L)}$			20	nsec	HI to SW, VB=48V, VCC=5V and 10A I_{OUT}
VCC Undervoltage-Lockout	$V_{CC,UVLO}$	3.8	4.0	4.2	V	
VCC Threshold Hysteresis	$V_{CC,HYS}$		0.35		V	
SW Rising Time	$T_{SW,R}$			2	nsec	VB=48V, F_{SW}=500kHz and 10A I_{OUT}
SW Falling Time	$T_{SW,F}$			4	nsec	

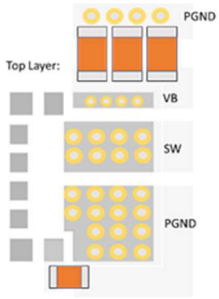
Application Specifications

VCC UVLO (Undervoltage-Lockout):

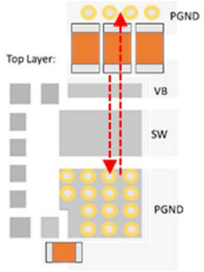
When VCC pin detects a starting threshold voltage level of 4.0V (typical) on a rising edge, the device will go from its 120uA quiescent current state to normal operation. The DrGaN will turn off after the input falls 0.35V below the starting threshold. A typical start-up waveform as below: (yellow: VB, blue: VCC and pink: SW)

PCB Layout Considerations：

- Thermal Enhanced ：Utilize multiple Via's to connect PCB power and GND planes to the DrGaN Pads, designer doesn't need to consider parasitic loop inductance issue to affect high voltage spike at SW node to decrease efficiency because RT10005SDH is designed with ultra-low commutation and gate loop inductance inside. An example PCB Layout as below：



- Dual Power Loop：For further reducing power loop parasitic inductance, PCB layout can consider another PCB layout skill that is to generate a power loop with magnetic flux cancellation plus a vertical power loop inside to achieve dual power design, the power loop inductance will be reduced from <1nH to <0.5nH. That will increase efficiency and decrease voltage spike at switching node. An example PCB layout as below：

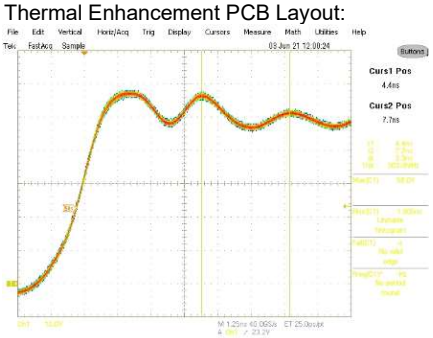


*Mid 1 layout MUST be power ground plane.

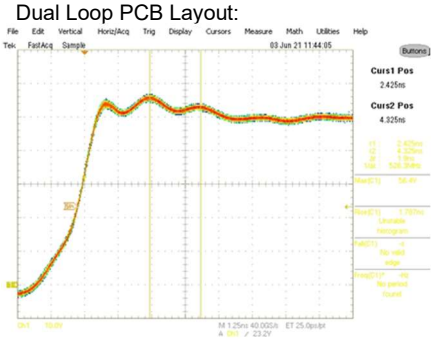
- Comparison the both PCB layout Skill：Thermal Enhancement can be handling more output current at the same environment and Dual Power Loop have better efficiency and voltage spike at SW node.

[a]. Rising Switching waveform: (Oscilloscope BW=1GHz)

Thermal Enhancement PCB Layout:

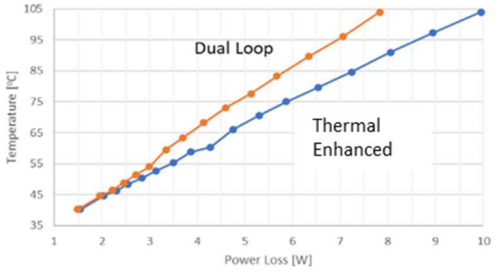


Dual Loop PCB Layout:

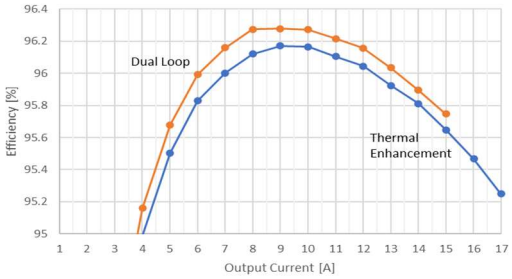


[b] Thermal performance and Efficiency between both PCB layouts

Thermal Performance: Thermal enhancement PCB layout have better thermal performance because of multiple Vias on SW pad.



Efficiency: Dual Loop PCB layout have better efficiency because of smaller voltage spike at SW node.



Full-Bridge or 3-phase operation

It easily be interleaved for Full-Bridge or 3-phase operation by using MCU/DSP with multiple PWM outputs and separate control loops.

Truth Table

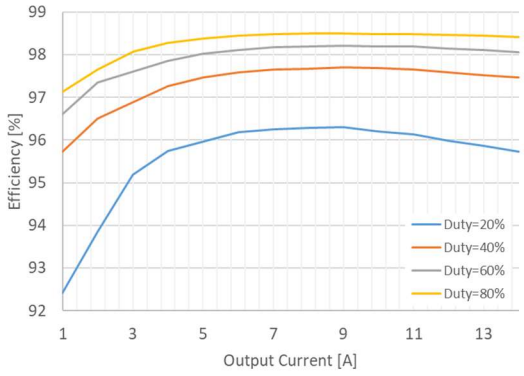
*Minimum H signal is 2.3V and Maximum L signal is 0.5V.

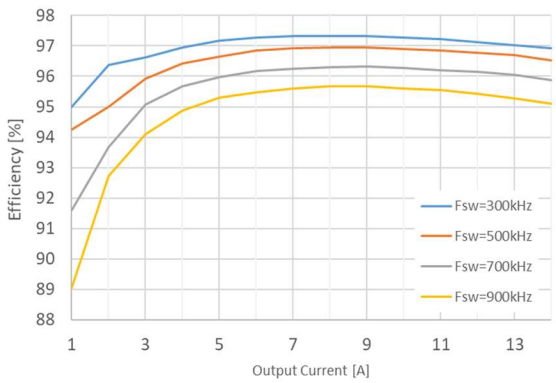
HI	LI	H/S GaN FET	L/S GaN FET	SW Node
L	L	OFF	OFF	Hi-Z
L	H	OFF	ON	GND
H	L	ON	OFF	VB
H	H	ON	ON	Not Allowed

Typical Efficiency and Switching Waveforms

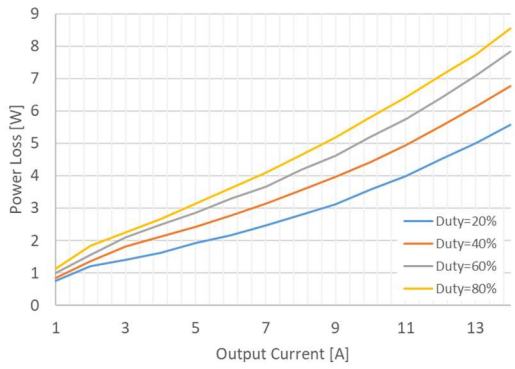
48V VB, Duty Cycle = 25%, F_{SW}=500kHz, I_{OUT} = 10A, 1GHz B.W. measurement, dead time is <15nsec, room temperature and natural convection. (All test is on the Evaluation Board)

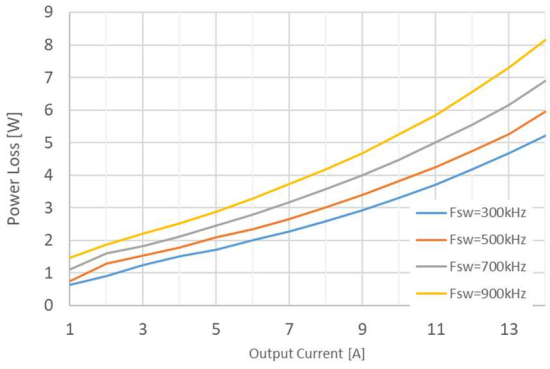
[1] Efficiency





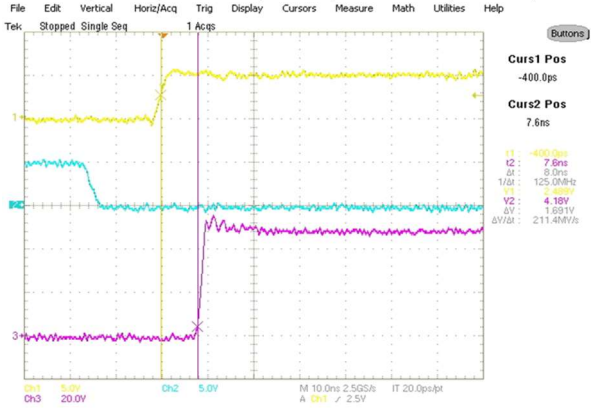
[2] Power Loss

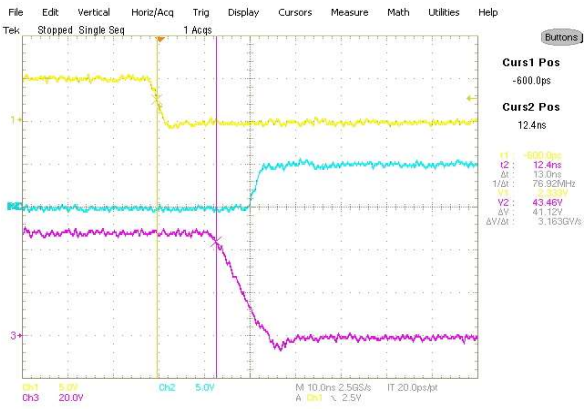




[3] Switching Waveforms

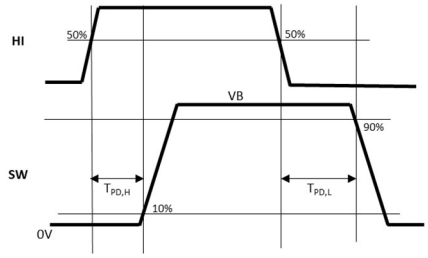
CH1: HI (5V/DIV), CH2: LI (5V/DIV), CH3: SW (20V/DIV)



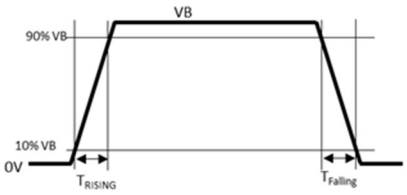


Propagation delay and rise/fall time definitions

a. Propagation Delay, $T_{PD,H}$ and $T_{PD,L}$

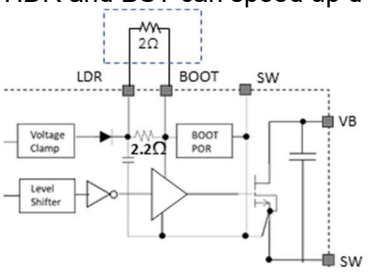


b. Rising/Falling Time, T_{Rising} and $T_{Falling}$

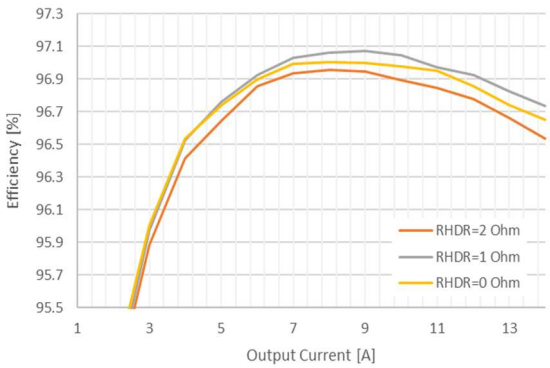


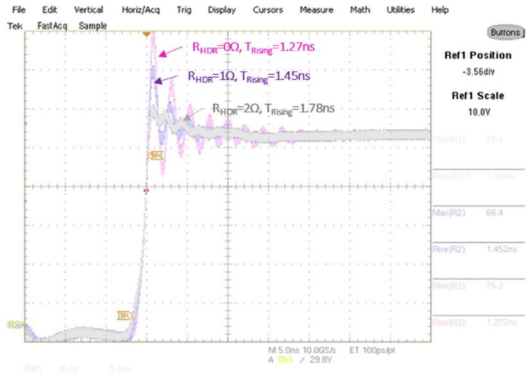
Adjustable Turn-on dV/dt Control

To reduce switching loss in high frequency hard switching operation, parallel a resistance between HDR and BST can speed up dV/dt at switching node to increase efficiency. R_{HDR} is designed =2Ω.



R_{HDR} value will change high side GaN's turned-on rising time, smaller R_{HDR} will cause faster turned-on time that will reduce switching loss, but higher voltage spike at SW node is also affect switching loss, R_{HDR}=2Ω is recommended if needs to fine-tune efficiency.





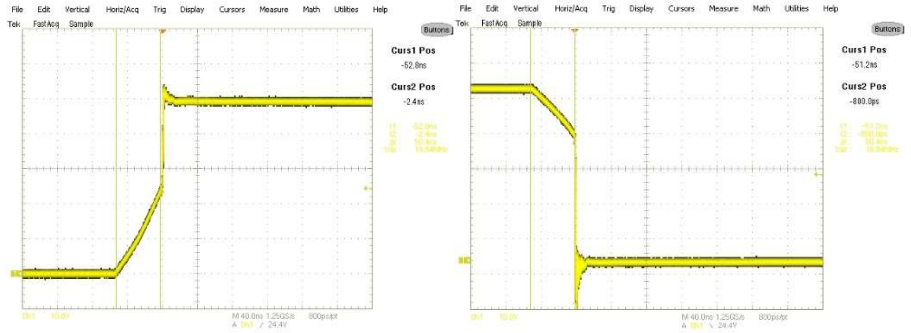
Dead time design and operation

• Typical Delay Matching Time is 1.5ns which limits minimum Dead Time to 1.5ns, however, **at least a 15ns Dead Time is recommended** for switching reliability. Additionally, the Dual PWM DrGaN has HI and LI PWM inputs, switching control is feasible especially in ZVS Mode and in Pulse Skip or power save mode during light load operation.

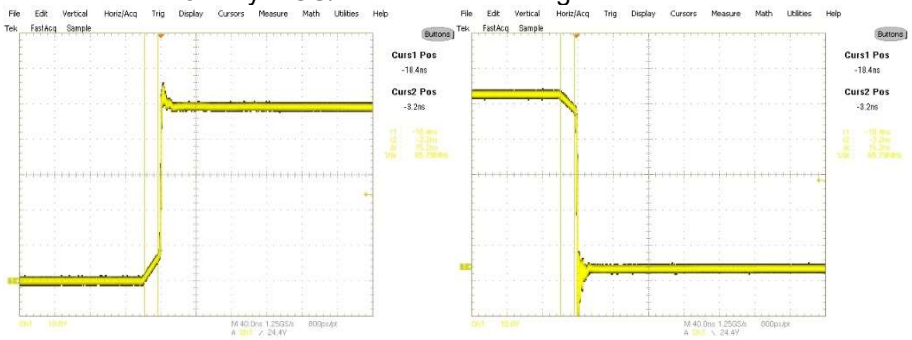
• In ZVS operation, controlling Dead Time low-to-high ($T_{DT,LH}$) can be achieved using output inductor and the C_{OSS} of the GaN Switch to generate a resonant period, using HI and LI to adjust $T_{DT,LH}$.

• Adjusting Dead Time

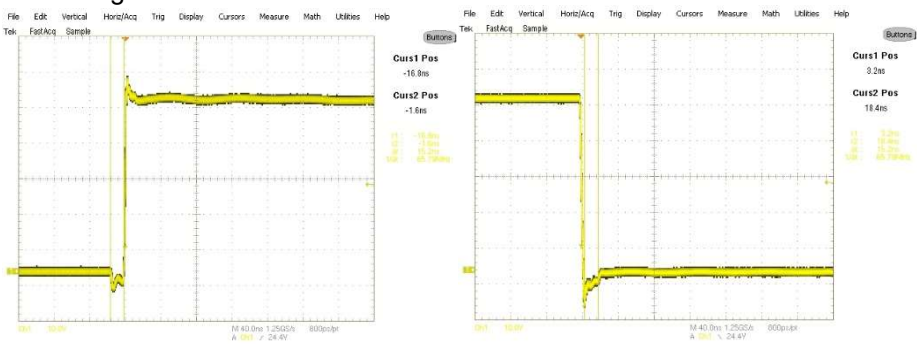
[1] Measure switch node to determine dead-time at no load. (Initial dead time can be set 50nsec by MCU/DSP or dead-time generator circuit in EVM)



[2] Reduce dead-time to > 15ns by MCU/DSP or dead-time generator circuit in EVM.

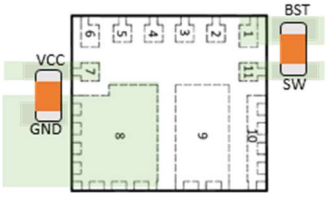


[3] Increase bus voltage and load.



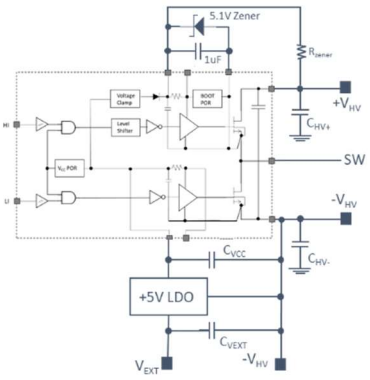
VCC Bypass Capacitor and V_{BST} Bootstrap Capacitor

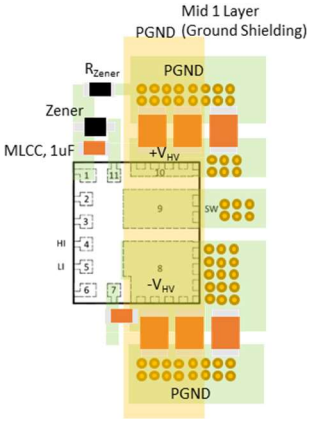
For lower switching frequency applications, likely BLDC Motor driver control, a typical switching frequency is from 20kHz to 50kHz. A 0.1-μF or larger value, good-quality, ceramic bypass capacitor is recommended to place as close as possible to the VCC and GND pins for low side driver supply and to the BST and SW pins for high side floating driver supply.



Implemented in the Class-D Amplifier Power Stage:

Due to GaN FET has much smaller Q_G and C_{OSS} than MOSFET that will produce a much more accurate PWM replication of the large output signal to increase sound quality in Class-D audio system. An example for half bridge Class-D audio amplifier schematic and recommended PCB layout are shown as below:



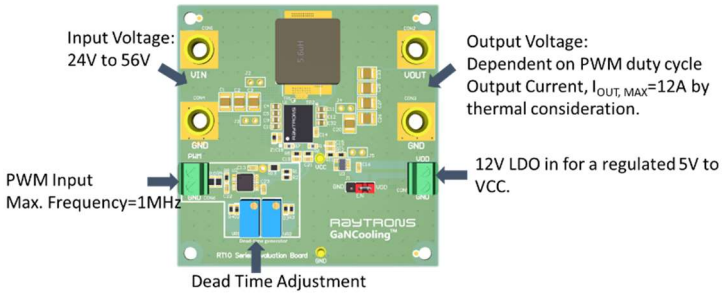


48V to 12V Open Loop Buck/Boost Evaluation Board:

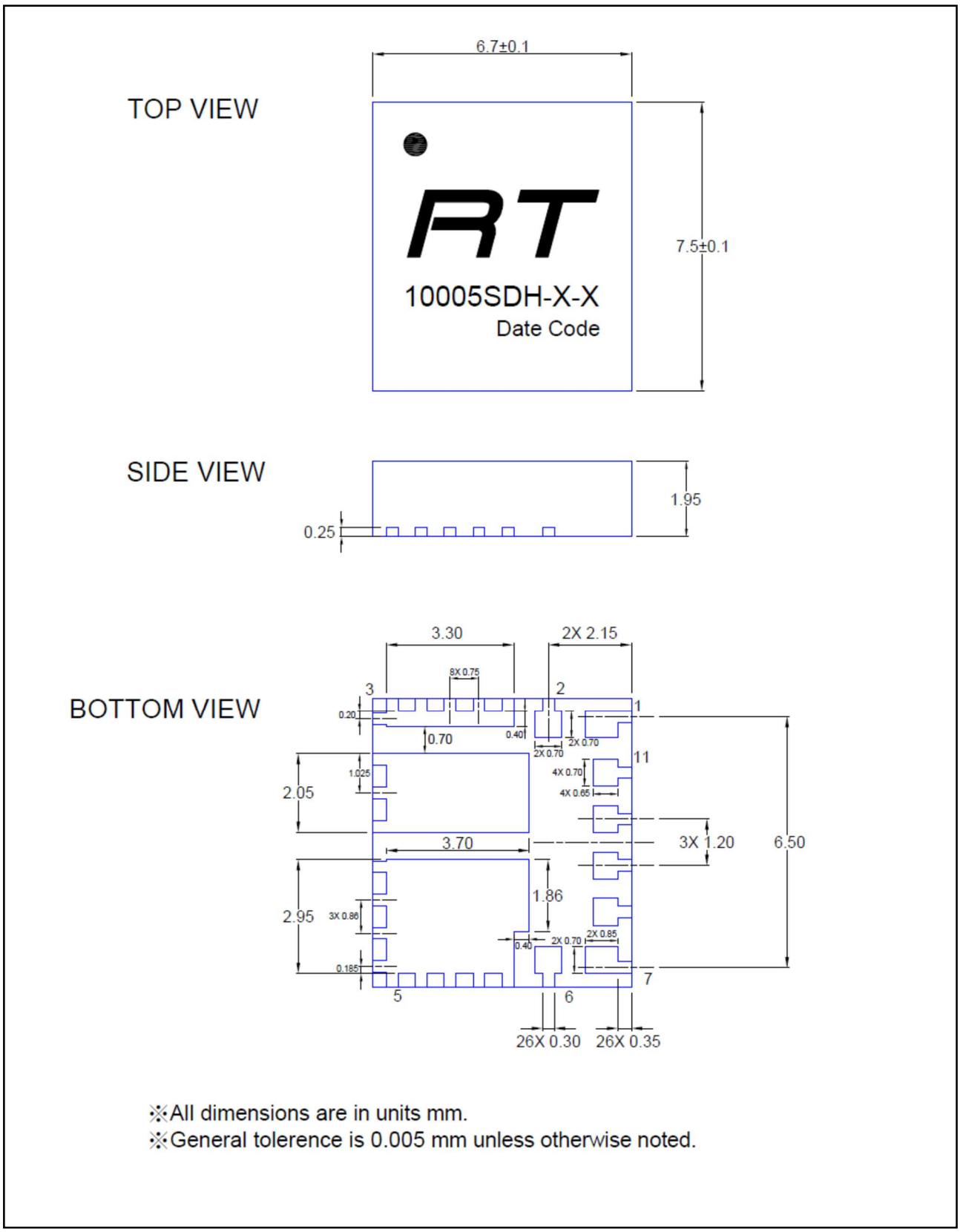
The Evaluation Board with 100V DrGaN SMT power stage provides a complete 48V step Up/down converter which can be used to evaluate efficiency & power density for use in applications such as DC/DC Converter power stage, high-performance Class D audio systems, and BLDC Motor Driver.

To evaluate the performance of the evaluation board, the following equipment is required:

- High speed digital oscilloscope (350MHz Bandwidth at least)
- DC load (power resistor or electrical load)
- DC power supplies *2 (For power in and VCC in)
- Signal generator for PWM input (0-5V)
- Current/Voltage Meters

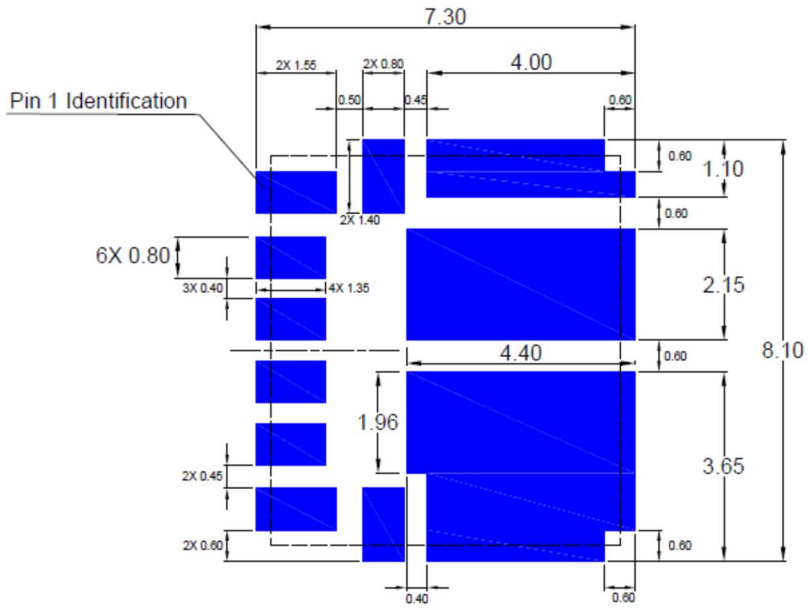


Package Outline： (QFN-SiP - 2 mm max height)

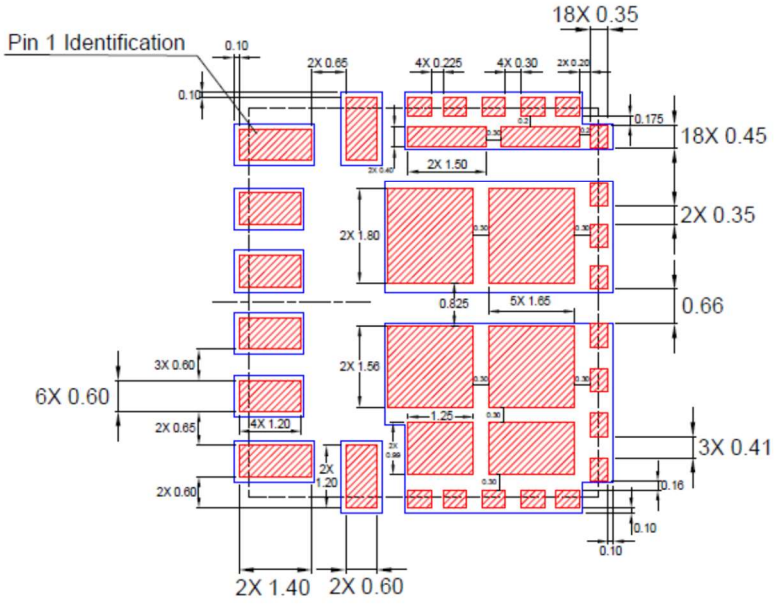


※All dimensions are in units mm.
※General tolerence is 0.005 mm unless otherwise noted.

Example Board Layout and Stencil Design：



RECOMMENDED LAND PATTERN



RECOMMENDED SOLDER PATTERN

※All dimensions are in units mm.
※53%~68% printed solder coverage by area under package.